8. A video signal control circuit as claimed in Claim 6, wherein the repetition processing or the deletion processing in the address generation circuit is executed to a rear part of the line of the input data.

9. A video signal control circuit as claimed in Claim 7, wherein the repetition processing or the deletion processing in the address generation circuit is executed to a rear part of the line of the input data.

10. A video signal control circuit as claimed in Claim 6, wherein the judgment circuit is able to set an initial value of the address generated by the address generation circuit in accordance with a selection signal.

11. A video signal control circuit as claimed in Claim 10, further comprising an initial value judgment circuit that judges an inclination of a pixel dispersion on the basis of the pixel number counted by the counter circuit, and outputs the selection signal that designates an initial value of the address in accordance with the inclination of the pixel dispersion.

12. A video signal control circuit as claimed in Claim 7, wherein the judgment circuit is able to set an initial value of the address generated by the address generation circuit in accordance with a selection signal.

13. A video signal control circuit as claimed in Claim 12, further comprising an initial value judgment circuit that judges an inclination of a pixel dispersion on the basis of the pixel number counted by the counter circuit, and outputs the selection signal that designates an initial value of the address in accordance with the inclination of the pixel dispersion.